In the Claims:

1. (Cancelled)

2. (Currently Amended) A ~~The~~ power amplifier configuration ~~of claim 1 further~~ comprising:

a) power control circuitry including a power regulator providing an output voltage at an output node responsive to an adjustable power control signal;

b) power amplifier circuitry including an input amplifier stage in series with an output amplifier stage for amplifying a radio frequency input signal, the output amplifier stage receiving power via the output node of the power regulator; and

c) bias circuitry for providing a constant bias to the input and output amplifier stages;

wherein the adjustable power control signal is adjusted to control output power provided by the power amplifier circuitry by controlling the voltage supplied to the output amplifier stage.

3. (Currently Amended) The power amplifier configuration of claim ~~1~~ 2 wherein the power regulator is a voltage regulator.

4. (Original) The power amplifier configuration of claim 3 wherein the power regulator is a linear closed loop voltage regulator.

5. (Currently Amended) A ~~The~~ power amplifier configuration comprising ~~of claim 1 wherein the power control circuitry further comprises~~:

a) power control circuitry comprising:

i) a power regulator providing an output voltage at an output node responsive to an adjustable power control signal;

~~a)~~ ii) an error amplifier having a first input for receiving the adjustable power control signal, a second input, and an output coupled to the

power regulator to control the output voltage at the output node; and

~~b)~~ iii) a feedback network coupled between the output node of the power regulator and the second input of the error amplifier; and

b) power amplifier circuitry including an input amplifier stage in series with an output amplifier stage for amplifying a radio frequency input signal, the output amplifier stage receiving power via the output node of the power regulator;

wherein the adjustable power control signal is adjusted to control output power provided by the power amplifier circuitry by controlling the voltage supplied to the output amplifier stage and the output of the error amplifier is responsive to both the adjustable power control signal and a voltage signal fed back from the output node of the power regulator.

6. (Currently Amended) A ~~The~~ power amplifier configuration ~~of claim 1 wherein the power amplifier circuitry further comprises~~ comprising:

a) power control circuitry including a power regulator providing an output voltage at an output node responsive to an adjustable power control signal; and

b) power amplifier circuitry including an input amplifier stage in series with an output amplifier stage for amplifying a radio frequency input signal, the output amplifier stage receiving power via the output node of the power regulator, the power amplifier circuitry further including a second output amplifier stage between and in series with the input and output amplifier stages, the second output amplifier stage receiving power via the output node of the power regulator such that the adjustable power control signal is adjusted to control output power provided by the power amplifier circuitry by controlling the voltage supplied to the output amplifier stage and the second output amplifier stage.

7. (Original) The power amplifier configuration of claim 6 wherein the bias circuitry further provides a constant bias to the second output amplifier stage.

8. (Cancelled)

9. (Currently Amended) A ~~The~~ mobile terminal ~~of claim 8 further~~ comprising:

a) a control system providing an adjustable power control signal to control output power for transmitted radio frequency signals;

b) communication electronics associated with the control system and comprising:

i) power control circuitry including a power regulator providing an output voltage at an output node responsive to an adjustable power control signal; and

ii) power amplifier circuitry including an input amplifier stage in series with an output amplifier stage for amplifying a radio frequency input signal, the output amplifier stage receiving power via the output node of the power regulator; and

c) bias circuitry for providing a constant bias to the input and output amplifier stages;

wherein the adjustable power control signal is adjusted to control output power provided by the power amplifier circuitry by controlling the voltage supplied to the output amplifier stage.

10. (Currently Amended) The mobile terminal of claim ~~8~~ 9 wherein the power regulator is a voltage regulator.

11. (Original) The mobile terminal of claim 10 wherein the power regulator is a linear closed loop voltage regulator.

12. (Currently Amended) A ~~The~~ mobile terminal ~~of claim 8 wherein the power control circuitry further comprises~~ comprising:

a) a control system providing an adjustable power control signal to control output power for transmitted radio frequency signals; and

b) communication electronics associated with the control system and comprising:

I i) power control circuitry comprising:

A) a power regulator providing an output voltage at an output node responsive to an adjustable power control signal;

B) ~~a)~~ an error amplifier having a first input for receiving the adjustable power control signal, a second input, and an output coupled to the power regulator to control the output voltage at the output node; and

C) ~~b)~~ a feedback network coupled between the output node of the power regulator and the second input of the error amplifier; and

ii) power amplifier circuitry including an input amplifier stage in series with an output amplifier stage for amplifying a radio frequency input signal, the output amplifier stage receiving power via the output node of the power regulator;

wherein the adjustable power control signal is adjusted to control output power provided by the power amplifier circuitry by controlling the voltage supplied to the output amplifier stage and the output of the error amplifier is responsive to both the adjustable power control signal and a voltage signal fed back from the output node of the power regulator.

13. (Currently Amended) A ~~The~~ mobile terminal ~~of claim 8 wherein the power amplifier circuitry further comprises~~ comprising:

a) a control system providing an adjustable power control signal to control output power for transmitted radio frequency signals; and

b) communication electronics associated with the control system and comprising:

i) power control circuitry including a power regulator providing an output voltage at an output node responsive to an adjustable power control signal; and

ii) power amplifier circuitry including an input amplifier stage in series with an output amplifier stage for amplifying a radio frequency input signal, the output amplifier stage receiving power via the output node of the power regulator, the power amplifier circuitry further including a second output amplifier stage between and in series with the input and output amplifier stages, the second output amplifier stage receiving power via the output node of the power regulator such that the adjustable power control signal is adjusted to control output power provided by the power amplifier circuitry by controlling the voltage supplied to the output amplifier stage and the second output amplifier stage.

14. (Original) The mobile terminal of claim 13 wherein the bias circuitry further provides a constant bias to the second amplifier output stage.

15. (Currently Amended) The mobile terminal of claim ~~8~~ 9 wherein the adjustable power control signal is V_{RAMP}.

16. (Cancelled)

17. (Currently Amended) A ~~The~~ semiconductor implementing a power amplifier configuration ~~of claim 16 further~~ comprising:

a) power control circuitry including a power regulator providing an output voltage at an output node responsive to an adjustable power control signal;

b) power amplifier circuitry including an input amplifier stage in series with an output amplifier stage for amplifying a radio frequency input signal, the output amplifier stage receiving power via the output node of the power regulator; and

c) bias circuitry for providing a constant bias to the input and output amplifier stages;

wherein the adjustable power control signal is adjusted to control output power provided by the power amplifier circuitry by controlling voltage supplied to the output amplifier stage.

18. (Currently Amended) The semiconductor of claim ~~16~~ 17 wherein the power regulator is a voltage regulator.

19. (Original) The semiconductor of claim 18 wherein the power regulator is a linear closed loop voltage regulator.

20. (Currently Amended) A ~~The~~ semiconductor implementing a power amplifier configuration ~~of claim 16 wherein the power control circuitry further comprises~~ comprising:

a) power control circuitry comprising:

i) a power regulator providing an output voltage at an output node responsive to an adjustable power control signal;

ii) ~~a)~~ an error amplifier having a first input for receiving the adjustable power control signal, a second input, and an output coupled to the power regulator to control the output voltage at the output node; and

iii) ~~b)~~ a feedback network coupled between the output node of the power regulator and the second input of the error amplifier; and

b) power amplifier circuitry including an input amplifier stage in series with an output amplifier stage for amplifying a radio frequency input signal, the output amplifier stage receiving power via the output node of the power regulator;

wherein the adjustable power control signal is adjusted to control output power provided by the power amplifier circuitry by controlling voltage supplied to the output amplifier stage and the output of the error amplifier is responsive to both the adjustable power control signal and a voltage signal fed back from the output node of the power regulator.

21. (Currently Amended) A ~~The~~ semiconductor implementing a power amplifier configuration ~~of claim 16 wherein the power amplifier circuitry further comprises~~ comprising:

a) power control circuitry including a power regulator providing an output voltage at an output node responsive to an adjustable power control signal; and

b) power amplifier circuitry including an input amplifier stage in series with an output amplifier stage for amplifying a radio frequency input signal, the output amplifier stage receiving power via the output node of the power regulator, the power amplifier circuitry further including a second output amplifier stage between and in series with the input and output amplifier stages, the second output amplifier stage receiving power via the output node of the power regulator such that the adjustable power control signal is adjusted to control output power provided by the power amplifier circuitry by controlling voltage supplied to the output amplifier stage and the second output amplifier stage.

22. (Original) The semiconductor of claim 21 wherein the bias circuitry further provides a constant bias to the second amplifier output stage.

23. (Cancelled)

24. (Currently Amended) A ~~The~~ method ~~of claim 23 further~~ comprising:

a) providing a regulated output voltage responsive to an adjustable power control signal;

b) providing an input amplifier stage in series with an output amplifier stage for amplifying a radio frequency input signal;

c) providing power to the output amplifier stage via the regulated output voltage; and

d) providing a constant bias to the input and output amplifier stages;

wherein the adjustable power control signal is adjusted to control output power provided by controlling voltage supplied to the output amplifier stage.

25. (Currently Amended) A ~~The~~ method ~~of claim 23 further~~ comprising:

a) providing a regulated output voltage responsive to an adjustable power control signal;

b) providing an input amplifier stage in series with an output amplifier stage for amplifying a radio frequency input signal;

c) providing power to the output amplifier stage via the regulated output voltage;

d) ~~a)~~ providing feedback from the regulated output voltage; and

e) ~~b)~~ generating a voltage control signal to control the regulated output voltage responsive to both the adjustable power control signal and feedback from the regulated output voltage;

wherein the adjustable power control signal is adjusted to control output power provided by controlling voltage supplied to the output amplifier stage.

26. (Currently Amended) A ~~The~~ method ~~of claim 23 wherein the amplifier circuitry further comprises~~ comprising:

a) providing a regulated output voltage responsive to an adjustable power control signal;

b) providing an input amplifier stage in series with an output amplifier stage for amplifying a radio frequency input signal;

c) providing power to the output amplifier stage via the regulated output voltage; and

d) providing a second output amplifier stage between and in series with the input and output amplifier stages, the second output amplifier stage receiving power via the output node of the power regulator such that the adjustable power control signal is adjusted to control output power provided by the power amplifier circuitry by controlling voltage supplied to the output amplifier stage and the

second output amplifier stage.

27. (Original) The method of claim 26 further comprising providing a constant bias to the second amplifier output stage.

28. (New) The power amplifier configuration of claim 2 wherein the input amplifier stage receives power from a fixed voltage node.

29. (New) The mobile terminal of claim 9 wherein the input amplifier stage receives power from a fixed voltage node.

30. (New) The semiconductor of claim 17 wherein the input amplifier stage receives power from a fixed voltage node.

31. (New) The method of claim 24 further comprising providing power to the input amplifier stage from a fixed voltage node.